Claim Amendments:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method comprising ~~the steps of~~:
identifying a first portion of multimedia data associated with video content;
identifying a second portion of the multimedia data associated with audio content, wherein the audio content is associated with the video content;
processing the first portion to generate video data;
processing the second portion to generate audio data;
transferring the audio data to memory in response to assertion of a first register portion; and
delaying ~~the~~ a transfer of audio data from memory to an audio output, wherein the delay is associated with a difference in a first time required to process the first portion to a second time needed to process the second portion;

2. (Currently amended) The method of claim 1 further comprising ~~the steps of~~:
providing the video data at a video output after the ~~step of~~ delaying a transfer.

3. (Original) The method as in Claim 1, wherein processing the first portion includes performing de-interlacing on the first portion.

4. (Original) The method as in Claim 1, wherein processing the first portion includes digitizing the first portion.

5. (Original) The method as in Claim 1, wherein processing the second portion includes digitizing the second portion.

6. (Original) The method as in Claim 1, wherein the delay is determined according to a mode of operation.

7. (Original) The method as in Claim 6, wherein the mode of operation includes receiving multimedia data associated with a broadcast analog audio and video program.

8. (Original) The method as in Claim 6, wherein the mode of operation includes receiving multimedia data associated with a broadcast digital audio and video program.

9. (Original) The method of claim 8, wherein the broadcast digital audio and video program is broadcast as part of a packetized multiplexed signal.

10. (Original) The method of claim 9, wherein the packetized multiplexed signal is an MPEG type signal.

11. (Original) The method as in Claim 6, wherein the mode of operation includes receiving multimedia data associated with picture-in-picture video to be generated, wherein a digital audio and video program is mixed with a representation of an analog video program.

12. (Original) The method as in Claim 6, wherein the mode of operation includes receiving multimedia data associated with picture-in-picture video to be generated, wherein an analog audio and video program is mixed with a representation of an analog video program.

13. (Currently amended) The method as in Claim 1, wherein ~~the step of~~ transferring includes transferring the audio data to audio memory using a first channel of a data port.

14. (Currently amended) The method as in Claim 11, wherein ~~the step of~~ transferring includes transferring the audio data to the audio output using a second channel of a data port.

15. (Currently amended) The method as in Claim 1, further including ~~the step of~~ adjusting a rate of transfer of the audio data to synchronize the audio data with the video data.

16. (Currently amended) A system comprising:

a data processor having an I/O buffer;

a memory having an I/O buffer coupled to the I/O buffer of the data processor, the memory storing code to control said data processor to:

determine a delay amount, wherein the delay is associated with a difference between an amount of time to process a portion of video data to amount of time to process a portion of audio data associated with the video data;

assert a transfer of processed audio data to memory through a data port;

assert, after waiting the delay amount, a transfer of a representation of the processed audio data from memory to an audio output through a data port;

a video processor to process the portion of video data to generate processed video data;

an audio processor to process the portion of audio data to generate processed audio data;

a memory controller comprising:

a first register ~~field~~ portion to enable a transfer of the processed audio data to memory; and

a second register ~~field~~ portion to enable a transfer of the representation of the processed audio data from memory to an audio output.

17. (Original) The system as in Claim 16, wherein said video processor further includes:

an analog video encoder to:

digitize analog video data to generate digital video data;

decode digital video data to analog video;

provide digital video data related to interlaced video data to a digital video processor;

provide the video data to the video output; and

said digital video processor to de-interlace digital video data related to interlaced video data.

18. (Original) The system as in Claim 17, wherein the digital video processor is to further process MPEG transport packets into video data.

19. (Original) The system as in Claim 16, wherein the audio processor is to further digitize analog audio data to digital audio data.

20. (Original) The system as in Claim 16, wherein the data port is coupled to the video processor.

21. (Original) The system as in Claim 16, wherein the data port is coupled to the video processor to transfer the processed audio data to and from memory.

22. (Original) The system as in Claim 16, further including a host bus interface unit, with an I/O bus coupled to the I/O bus of the data processor, to provide access to memory to the data port.

23. (Original) The system as in Claim 16, wherein the delay is determined according to a mode of operation.

24. (Original) The system as in Claim 23, wherein the mode of operation includes processing multimedia data associated with analog audio and video content to generate the portion of audio data and the portion of video data.

25. (Original) The system as in Claim 23, wherein the mode of operation includes processing multimedia data associated with digital audio and video content to generate the portion of audio data and the portion of video data.

26. (Original) The system as in Claim 23, wherein the mode of operation includes generating picture-in-picture video data by mixing multimedia data associated with digital audio and video content with video data associated with an analog video content.

27. (Original) The system as in Claim 23, wherein the mode of operation includes generating picture-in-picture video data by mixing multimedia data associated with analog audio and video content with video data associated with an analog video content.

28. (Original) The system as in Claim 16, wherein memory is to further store code to:

assign a first address associated with a first portion of memory to store processed audio data;

assigning a second address associated with a second portion of memory to read a set of a representation of the processed audio data.

29. (Original) The system as in Claim 28, wherein a rate of transfer of processed audio data is altered to keep an amount of stored data between the first and second addresses constant.

30. (Original) The system as in Claim 16, wherein the data port is a multiple channel data access port and further includes:

a first FIFO channel for transferring the processed audio data to memory; and

a second FIFO channel for transferring the representation of the processed audio data from memory.

31. (Original) The system as in Claim 30, further including a third FIFO channel for performing general functions.

32. (Original) The system as in Claim 31, wherein the first and second port include separate controls for initiating data transfers.

33. (Currently amended) A computer readable medium tangibly embodying a plurality of instructions, the plurality of instructions for:

storing a delay amount, wherein the delay amount is associated with a difference between an amount of time to process a portion of video data to the amount of time to process a portion of audio data, wherein the portion of audio data is associated with the video data;

assigning a first address associated with a portion of memory to write a set of processed audio data;

assigning a second address associated with a portion of memory to read a set of stored audio data, wherein the stored audio data is associated with the processed audio data;

asserting a transfer of processed audio data to memory through a data port in response to assertion of a register portion, wherein the transfer implements the delay amount.

34. (Original) The computer readable medium as in Claim 33, further including adjusting a rate of transfer of stored audio data to maintain a constant amount of data between the first and the second addresses.

35. (Original) The computer readable medium as in Claim 33,wherien the computer readable medium is coupled to controls of the data port.

36. (Original) The computer readable medium as in Claim 33, further including determining the delay by analyzing presentation times associated with the portion of audio data and the portion of video data.